BRIEF INTRODUCTION TO DEEP LEVEL TRANSIENT SPECTROSCOPY

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Abstract: *Deep Level Transient Spectroscopy DLTS belong to capacitance transient thermal scanning method used for observing deep impurities and defect states in semiconductor* [1]. *Deep levels introduced near the middle of the energy gap by strong localized imperfections* [2], *are probably the main reason for impair the properties of High Electron Mobility Transistors (HEMT): gate-lag, drain-lag and virtual gate. DLTS method allows finding non-radiative recombination point defects in semiconductors, which could influence the carrier properties between the areas below the gate electrode and drain electrode. DLTS method gives the information about the energy level, concentration, thermal emission rate and the capture cross section of each trap. This technique cooperate quite well with luminescence, which allows observing shallow centers localized near the edge of valance or conduction band. In this paper will presented, the fundamental physical description of transition process in semiconductor, the basic results of DLTS measurements and the conclusions.*

Keywords: DLTS, point defect, HEMT

1. INTRODUCTION

Defects have influence at properties of many semiconductor devices; these introduced intentionally called impurities are inherent part in semiconductor devices fabrication and these existing in semiconductor material are frequently responsible for many parasite effects, such as the gate-lag, drain-lag, current collapse, current suppression, negative differential resistance and kink effect. For the main reason of this negative phenomena's very often imputes traps of carriers at surface or in bulk [3]. In the following chapters will be present, the fundamental physical description of transition process in semiconductor. The basic comparison of DLTS measurements at intentionally doped BSX61 switching transistor BSX61 with BC211 low power transistor and the conclusion.

2. TRANSITION PROCESS

Defect states existing in semiconductor materials are localize inside the forbidden gap, impurities like donor or acceptors, are shallow defects, they lie near the edge of the valence and of the conduction bands. On the other hand, deep defects are localize at the middle of the forbidden gap. Deep defects are atoms that lie at interstitial position they cannot replace lattice atoms in semiconductor materials. Figure 1. (left) presented a deep defect in the silicon crystalline lattice. Au atoms interact with nearest silicon atoms and with the free electrons. The probability of capture free electron by deep defect are much higher than his recombination directly to the valence band. To the main transition process should be taken into account; the electron emission g_e the electron capture k_e the hole emission g_h and the hole capture k_h by Au atoms, presented in Figure 1. (right) as the band diagram. The trap

level with energy E_T is localize near the middle of the forbidden gap. The conduction band E_c with free electrons lie above the trap level and the valence band E_V with valence electrons lie under the trap level.

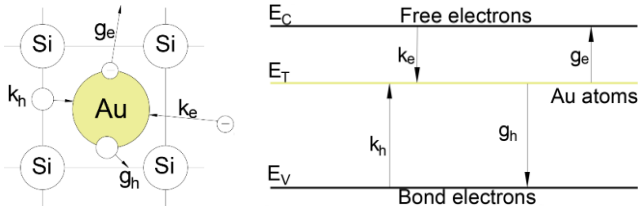

Fig. 1. The deep interstitial gold defect inside silicon lattice (left). The simplified band diagram of transitions: the electron emission g_e the electron capture k_e the hole emission g_h and the hole capture k_h (right)

The probability of capture an electron from the conduction band by deep defect in function of time is [4]:

$$k_e = \sigma_n v_n N_C \gamma \exp\left(-\frac{E_c - E_T}{k_B T}\right) \tag{1}$$

Comparing the kinetic energies and treating the electrons like particles with three degrees of freedom, the thermal velocity of electrons in function of temperature could be obtain [5, 6]:

$$\frac{1}{2} m v_e^2 = \frac{3}{2} k_B T \rightarrow v_e \sim \sqrt{T} \tag{2}$$

Assuming that all free electrons are localize near the conduction band the effective density of states [7] in function of temperature is:

$$N_c = 2\left(\frac{2\pi m_n k_B T}{(2\pi\hbar)^2}\right)^{\frac{3}{2}} \rightarrow N_c \sim T^{\frac{3}{2}} \tag{3}$$

Capture cross section for electrons σ_n and the degeneracy factor γ also changes with temperature, the equation (1) looks now:

$$k_e = \sigma_n(T)\, T^2 A \exp\left(-\frac{\Delta E}{k_B T}\right) \tag{4}$$

where: A is constant that not change with the temperature.

3. EXPERIMENTAL RESULTS

Emission rate is the time needed to achieve thermal equilibrium by carriers that intentionally have been introduce to non-equilibrium state. To determine the emission rate of the trap levels in test switching transistor BSX61 it is essential to provide non-equilibrium condition by "injected pulse" V_F that inject the carriers into the depleted region. Next applying the reverse bias V_R to measure the difference between the capacitance of base-emitter junction BSX61 switching transistor C and compensated capacitance C_0, $\Delta C = C - C_o$, presented at Figure 2. After the injected pulse, the width of the depleted region will decrease and majority carriers starts to diffuse, in results the capacitance of depleted region will change.

Under the reverse bias the width of the barriers increase and only the generation and minority carrier's current will occurs. The system will back to the equilibrium state before the next injected pulse the capacitance in depleted region will return to the initial value. The time for measuring the capacitance i.e. the time for applying the reverse bias is set for 200 ms and the time for injected pulse is set to 1 ms.

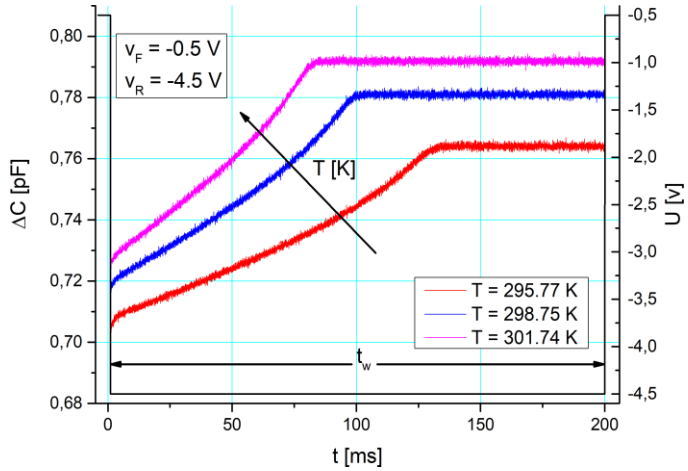

Fig. 2. Capacitance and applied voltage of base-emitter junction in BSX61 switching transistor for three different temperatures. Reverse voltage was applied for $t_w = 200$ ms

The capacitance transient are measured for wide range of temperatures and using the lock-in method (equation 5) DLTS signal presented at Figure 5 could be obtain:

$$S_{DLTS} = \int_{t\prime}^{2t\prime} \Delta C dt - \int_{0}^{t\prime} \Delta C dt \,;\; t' = \frac{t_w}{2} \tag{5}$$

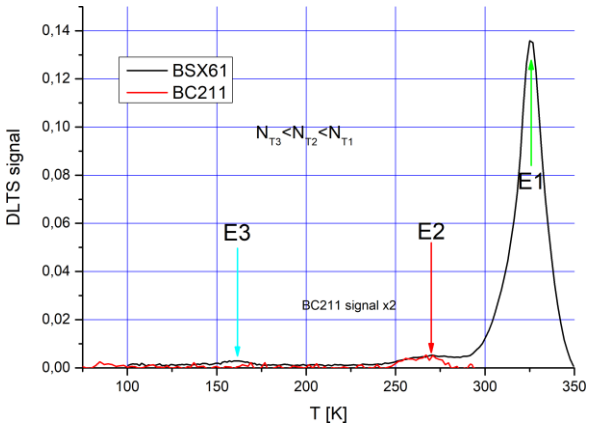

Fig. 3. DLTS signal for Si: BSX61 switching transistor (black) and Si: BC211 low power transistor (red), window width $t_w = 200$ ms. DLTS signal for BC211 was multiplied by 2

At Figure 3., three kinds of traps in BSX61 switching transistor are observe. The intensity of DLTS signal corresponds to trap concentration. The first trap level is active in temperatures from 150 K to 170 K the second trap level is active from 250 K to 370 K and the third from 300 K to 360 K. To determine the trap energies and the capture cross sections the inverted Laplace transform (equation 6) for each transients have to be involve.

$$f(t) = \int_0^\infty F(s)\exp(-st)dt \tag{6}$$

In result, receive the spectrum of exponents and peaks corresponds to the emission rate of carriers from different trap levels (Figure 4).

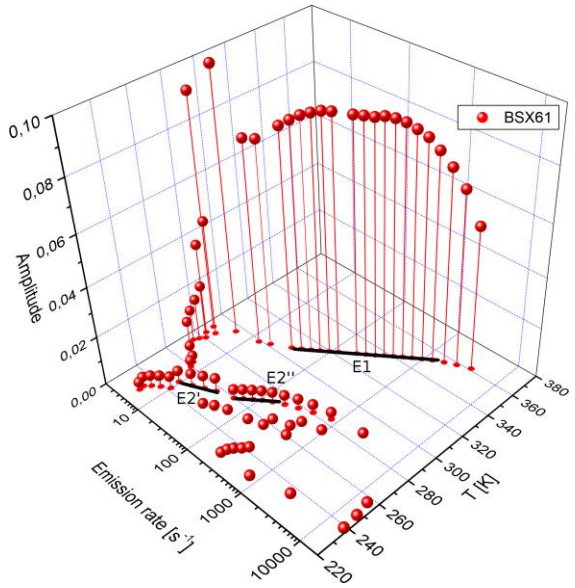

Fig. 4. Amplitude and emission rate following the Laplace transform applied to capacitance transients in wide range of temperatures. Three traps levels are observe E1 in temperature range from 300 K to 360 K temperatures and E2' with E2'' in temperature range from 220 K to 260K

Rewriting, the equation (4) in the straight-line form $y = ax + b$ the basic quantities could be obtain.

$$\ln\frac{g_n}{T^2} = -\Delta E\frac{1}{k_B T} + \ln\eta\sigma_n \tag{7}$$

The slope of the curve is equal to energy of the trap level and the intercept respond for the capture cross section. The Arrhenius plot for the first deep trap is present at Figure 5.

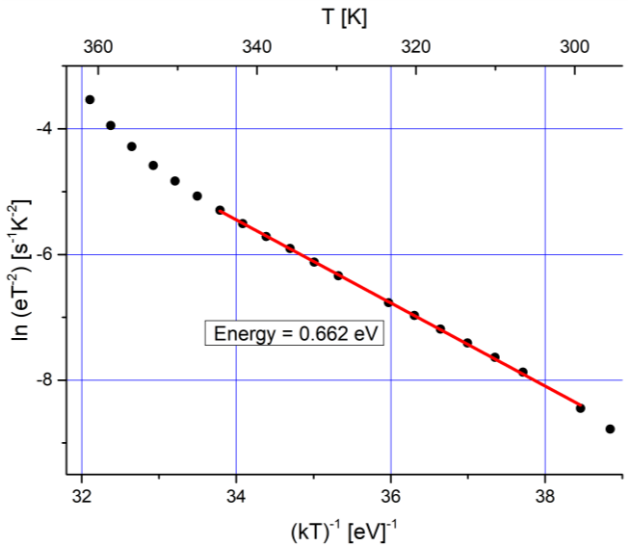

Fig. 5. Arrhenius plot of the first defect (equation 7) in switching transistor Si: BSX61, the curve determined by linear combination of emission rate peaks obtained from inverted Laplace algorithm

4. CONCLUSIONS

In this paper was present the basic physical and experimental concept of the Deep Level Transients Spectroscopy to determining deep defects in semiconductor materials. The measurements was make at the switching transistor BSX61 and BC211 low power transistor. From the data presented at Figure 5, the energy of E1 defects could be estimate. The E1 deep defect lies 0.662 eV below the conduction band. Energy equal to 0.662 eV match very well with the Mn atoms from the literature [8]. The deep traps in intentionally doped BSX61 switching transistor was detect by Laplace DLTS system are responsible for reducing the minority carrier lifetime in base, thereby for reducing the storage time. Non-doped BC211 low power transistor possess very low concentration of deep defects undetectable by typical Laplace a DLTS measurements.

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